Memory RAS Trends – OCP Fleet Memory Fault Management Framework

Server operators do not have the required device-specific knowledge to understand memory errors and to determine how to react to them.  The industry desires a framework for gathering error data from memory, analyzing the data, determining when memory is at risk of causing crashes or performance issues and determining the best course of action to mitigate the memory error, including defining and driving RAS actions such as PPR, page offline, and other mitigations such as replacing DIMMs.

In mid-2023, the OCP Fleet Memory Fault Management (FMFM) workstream began. The OCP Memory Fault Management (FMFM) group has developed an initial specification for the standardization of memory error collection and in-field failure mitigation by incorporating vendor intelligence, including error decoder and fault analyzer from CPU vendor and memory vendor. The workgroup has incorporated input from memory vendors, CPU vendors, Cloud Service Providers, OEMs, and System Integrators.

The specification includes standardized data collection practices and formatting related to memory error, allowing low-overhead implementation for server operations, CPU vendor and memory vendors alike. This enables the most optimal RAS actions and greatly reduces memory-related server downtime in fleet operation by better utilizing CPU vendors’ platform RAS knowledge and memory vendors’ DRAM-specific knowledge. This standardization also drives efficiencies for DRAM vendors by enabling more efficient and standardized data collection. This results in improved turnaround time for failure analysis and manufacturing and design improvements.

The following diagram illustrates how FMFM framework are integrated into a single Vendor-Specific Fault Analyzer (VSFA).

